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10/591,390	09/01/2006	Pieter Van Der Wolf	NL04 0206 US1	8116

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NXP, B.V.
NXP INTELLECTUAL PROPERTY & LICENSING
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
LEE, ANDREW CHUNG CHEUNG	
ART UNIT	**PAPER NUMBER**
2419	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/591,390	VAN DER WOLF ET AL.	
	Examiner	Art Unit	
	Andrew C. Lee	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4-9,11-15* is/are rejected.

7)☒ Claim(s) *3 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Claims 13 – 15 are newly added.

Claims 1 – 15 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 2, 4 – 9, 11 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada (US 6871001 B1) in view of Linzer (6091776).

Regarding claims 1, 11, 12, Okada discloses a video stream processing circuit (Fig. 1), and a method of video stream processing *(Abstract, Fig. 1, col. 6, lines 24 – 38)*, comprising: signal processing circuitry arranged to execute a first video stream processing function *("MPEG decode core circuit"; Fig. 1, col. 7, lines 60 – 66);* a first and second buffer memory coupled to the signal processing circuitry, for buffering the frame data produced by the first video stream processing function, the first buffer memory being coupled to the signal processing circuitry via a shareable channel, the signal processing circuitry having access to the second buffer memory outside the shareable channel *("first frame buffer", and "second frame buffer"; Fig. 1, col. 6, lines 24 – 38);* wherein the first video stream processing function comprises writing frame data

of successive video frames in a temporally ordered output sequence of frames into the first and/or second buffer memory *(col. 6, lines 52 – 55, col. 8, lines 29 – 32)*; the signal processing circuitry being arranged to execute a second video stream processing function using the written frame data in a temporally ordered input sequence of frames that differs from the output sequence, the second video stream processing function, the first video stream processing function being arranged to select to read the frame data of predetermined first and second ones of the frames selectively from the first and second buffer memory respectively ("decoding…first frame buffer…..second frame buffer…"; col. 6, lines 49 – 59, col. 8, lines 63 – 67, col. 9, lines 1 – 12), except the second ones of the frames occurring in the same temporal order in both the input and output sequence, the first ones of the frames containing at least all particular frames whose position relative to the second ones of the frames in the output sequence differs from the position of the particular frames relative to the second ones of the frames in the input sequence. Linzer in the same field of endeavor teaches except the second ones of the frames occurring in the same temporal order in both the input and output sequence, the first ones of the frames containing at least all particular frames whose position relative to the second ones of the frames in the output sequence differs from the position of the particular frames relative to the second ones of the frames in the input sequence *(Fig. 2, col. 2, lines 58 – 67, col. 3, lines 1 – 9).*

At time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the teachings of Okada to include the features of the second ones of the frames occurring in the same temporal order in both the input and

output sequence, the first ones of the frames containing at least all particular frames whose position relative to the second ones of the frames in the output sequence differs from the position of the particular frames relative to the second ones of the frames in the input sequence as taught by Linzer. One of ordinary skill in the art would be motivated to do so for providing encoding video signals so as to achieve a truly constant encoding to decoding delay *(as suggested by Linzer, see col. 1, lines 18 – 20).*

Regarding claim 2, Okada discloses the video stream processing circuit claimed, comprising a first integrated circuit, which comprises the signal processing circuitry and the second buffer memory, and a second, separate integrated circuit that comprises the first buffer memory, the shareable channel forming part of a connection between the first and second integrated circuit *(Fig. 1, col. 7, lines 60 – 66).*

Regarding claim 4, Okada discloses the video stream processing circuit claimed wherein the first video stream processing function includes an MPEG decoding function, the first ones of the frames including at least decoded MPEG P-frames, the MPEG decoding function reading frame data from decoded MPEG I-frames and decoded MPEG P frames from the first buffer memory *("I-picture", "P-picture"; col. 13, lines 20 – 25).*

Regarding claim 5, Okada discloses the video stream processing circuit claimed wherein the second ones of the frames include B frames *("B-picture"; col. 9, lines 25 – 29).*

Regarding claim 6, Okada discloses the video stream processing circuit claimed wherein the signal processing circuitry writes B frames to the second buffer memory only *("B-picture"; col. 4, lines 2 – 3, col. 9, lines 25 – 29).*

Regarding claim 7, Okada discloses a video stream processing circuit claimed wherein the second ones of the frames include I frames, the first video stream processing function writing copies of the I frames to both the first and second buffer memory *(col. 9, lines 20 – 25).*

Regarding claim 8, Okada discloses the video stream processing circuit claimed wherein the second ones of the frames include B frames *(col. 9, lines 8 – 12).*

Regarding claim 9, Okada discloses a video stream processing circuit claimed wherein the first video stream processing function comprises an MPEG decoding function, the second video stream processing function reading at least decoded MPEG P-frames from the first buffer memory *(col. 9, lines 13 – 25).*

4. Claims 13, 14, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada (US 6871001 B1) and Linzer (6091776) as applied to claims 1, 11, 12 above, and further in view of Matsutani et al. (US 7408587 B2).

Regarding claims 13, 14, 15, Okada and Linzer do not disclose explicitly wherein the second buffer memory has a capacity of less than one frame.

Matsutani et al. in the same field of endeavor teach explicitly wherein the second buffer memory has a capacity of less than one frame *("the second buffer memory having a capacity corresponding to at least half of one frame"; col. 5, lines 55 – 59).*

At time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the teachings of Okada and Linzer to include the features of wherein the second buffer memory has a capacity of less than one frame as taught by Matsutani et al. One of ordinary skill in the art would be motivated to do so for providing a data conversion circuit for converting a component array, etc. of image data in an image processing device such as a digital camera *(as suggested by Matsutani et al., see col. 1, lines 9 – 11).*

Allowable Subject Matter

5. Claims 3, 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed on 4/07/2009 with respect to claims 1 – 15 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claim 1, applicant argues although Okada discloses generating a video signal from data written into the frame buffers (104a) and (104b), it is silent as to the relationship between the sequence in which the data was written into the frame

buffers and the sequence in which the data was subsequently read from the frame buffers. In particular, Okada fails to disclose that the display circuit (107) reads frames from one of the frame buffers (104a) and (104b) in, which sequence in time is the same sequence in time as the frames were written into the frame buffer. Okada also fails to disclose that the display circuit (107) reads frames from the other frame buffer of the frame buffers (104a) and (104b) in a sequence in time, which sequence in time is different from the sequence in time as the frames were written into the frame buffer. Accordingly, Okada fails to disclose the above-identified limitations of claim 1.

In response to the applicant's remark, Examiner respectfully disagrees. Examiner contends the combined system of reference Okada and newly found reference Linzer teaches the display circuit (107) reads frames from one of the frame buffers (104a) and (104b) in, which sequence in time is the same sequence in time as the frames were written into the frame buffer. Okada also fails to disclose that the display circuit (107) reads frames from the other frame buffer of the frame buffers (104a) and (104b) in a sequence in time, which sequence in time is different from the sequence in time as the frames were written into the frame buffer *(see Linzer, Fig. 2, col. 2, lines 58 – 67, col. 3, lines 1 – 9).*

Regarding claim 3, Applicant's arguments, see page 11, with respect to claim 3 have been fully considered and are persuasive. The rejection of claim 3 has been withdrawn.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Yavits et al. (US 6690726 B1).
b) Cheney et al. (5668599).
c) Kato (US 6785464 B1).
d) Nallur et al. (US 20030123849 A1).
e) Itoh Et al. (US20060165387 A1).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Lee whose telephone number is (571)272-3131. The examiner can normally be reached on Monday through Friday from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew C Lee/
Examiner, Art Unit 2419
<6/15/2009::3Qy09>
/Ayaz R. Sheikh/
Supervisory Patent Examiner, Art Unit 2419